

GNERFET BASED 8-BIT ALU

H.V. RAVISH ARADHYA¹, MADAN H R², MEGARAJ T M³, SURAJ M S⁴, KARTHIK R K⁵, MUNIRAJ R⁶

¹R V College of Engineering, Mysore Road, Bengaluru, Karnataka, India

²Chhattisgarh Swami Vivekanand Technical University, Bhilai, Chhattisgarh, India

^{3,4,5,6}R V College of Engineering, Mysore Road, Bengaluru, Karnataka, India

ABSTRACT

The advancement in IC technology rendering area optimized and fast ICs is primarily attributed to MOSFET scaling theory. The scaling theory sustained the Moore's law till the channel size reached the nano-meter regime. The issues in MOSFET due to scaling aggregated and resulted in leakage currents and high power dissipation making the transistor unreliable. The research has been done to find a potential replacement for traditional CMOS and to sustain Moore's law. Many alternatives like

CNTFET and FINFET based designs were found, but Graphene Nano Ribbon (GNERFET) based design was found to be more viable option in terms of area and power dissipation. Thus analysis of the circuits built using GNERFET is necessary to demonstrate its merits. The paper describes the design of GNERFET based 8-bit ALU and its comparison with conventional CMOS design with respect to power consumption, showing 0.1589 μ W for GNERFET based design and 15.57 μ W for CMOS design. For the design, 10nm process technology was used for GNERFET and conventional CMOS designs.

KEYWORDS: CMOS, GNERFET ALU, Power Dissipation